AMENDMENTS TO THE CLAIMS:

The listing of claims will replace all prior versions, and listings of claims in the application:

LISTING OF THE CLAIMS

1. (Currently Amended) A decoder comprising:

~~a~~ an SISO device that operates as a PCCC decoder in a first mode of operation and as an SCCC decoder in a second mode of operation where the device operates as per at least one trellis using an ~~in-line~~in-place addressing technique to process information.

2. (Currently Amended) The ~~processor~~ decoder of claim 1 where the device processes information in accordance with an algorithm.

3. (Currently Amended) The ~~processor~~ decoder of claim 2 where the algorithm is a Log MAP algorithm and the SISO device is a Log MAP processor.

4. (Currently Amended) The ~~processor~~ decoder of claim 1 where in the first mode of operation the SISO device operates as a first SISO during one time period and in the second mode of operation operates as a second SISO device during a second time period where the first and second SISO devices process information as per the same or different trellis.

5. (Currently Amended) The ~~processor~~ decoder of claim 1 where in the second mode of operation the SISO device operates as an inner SISO during one time period whereby it processes information as per a first trellis and operates as an outer SISO during another time period whereby it processes information as per a second trellis.

6. (Currently Amended) The ~~processor~~ decoder of claim 5 where the first trellis is a N_1-state Radix-K trellis and the second trellis is a N_2-state Radix-K trellis

where N_1 may or may not be equal to N_2 and K, N_1 and N_2 are integers equal to 1 or greater.

7. (Currently Amended) The ~~processor~~ decoder of claim 1 where the SISO ~~processor~~ device comprises:

at least one branch metric calculator;

at least one forward path metric calculator and at least one backward path metric calculator where both calculators are in communication with the branch metric calculator;

at least one Log Likelihood calculator coupled to the path metric calculators; and

at least one subtractor circuit having an extrinsic information input and coupled to the at least one Log Likelihood calculator to provide at least one Log Likelihood ratio output whereby the path metric calculators and the at least one Log Likelihood calculator are constructed with Log Sum operators which are designed based on an approximation of a Jacobian definition of a Log Sum operation.

8. (Currently Amended) The ~~processor~~ decoder of cliam 7 in which the information is processed as per an N_1 state Radix-K first trellis and an N_2 state Radix-K second trellis when operating as an SCCC turbo decoder where N_1 is not equal to N_2 and where N_1 and N_2 are integers equal to 2 or greater and K is an integer equal to 4 or greater.

9. (Currently Amended) The ~~processor~~ decoder of claim 7 where the SISO ~~processor~~ device is operating as a PCCC decoder and N_1 ~~may not be~~is equal to N_2 and K is an integer equal to 4 or greater and N_1, N_2 are integers equal to 2 or greater.

10. (Currently Amended) The ~~processor~~ decoder of claim 1 where the ~~in-line~~in-place addressing technique uses a block of memory for retrieving and storing values of the states of the trellis as the device processes the received information.

11. (Currently Amended) The ~~processor~~ decoder of claim 1 where information is processed using a portion of the states of the trellis to perform the ~~in-line~~in-place addressing technique during a clock cycle.

12. (Currently Amended) A method of performing turbo decoding, the method comprising the step of:

processing, in accordance with an algorithm, received information as per an N-state Radix-K trellis using an ~~in-line~~in-place addressing technique where N, K are ~~integer~~ integers equal to 1 or greater.

13. (Currently Amended) The method of claim 12 where the received information is processed as per an N-state Radix-K trellis using an ~~in-line~~in-place addressing technique where N is an integer equal to 2 or greater and K is an integer equal to 4 or greater.

14. (Currently Amended) The method of claim 12 where the ~~in-line~~in-place addressing technique uses a block of memory to retrieve and store states of the trellis as information is processed per the trellis.

15. (New) A decoder comprising:

an interleaver;

a deinterleaver; and

a soft input soft output device in communication with the interleaver and the deinterleaver, the soft input output device being operative to use an in-place addressing techniques when processing path metric data related to each of the states of a trellis , whereby a block of memory storing the path metric data is sequentially processed in a plurality of equally sized groups in accord with a trellis processing algorithm , and whereby when data from a selected one of the groups is read from an associated group of memory locations in a current pass of the trellis processing algorithm, those memory locations are made available to receive and store output data from the trellis processing algorithm, and whereby output data from the trellis processing algorithm that is appropriately stored in memory locations of the selected

group is stored in memory locations of the selected group and output data that is appropriately stored in a memory location of a second group, from which data has not been yet been read in the current pass of the trellis processing algorithm, the output data that is appropriately stored in a memory location of the second group is stored in a hold register and whereby when data from the second group is read from the associated second group of memory locations, those memory locations are made available to receive and store output data from the trellis processing algorithm and appropriate data from the hold register is copied into the newly available appropriate memory locations associated with the second group, whereby the same block of memory is used to store input data to the trellis processing algorithm and output data from the trellis processing algorithm and whereby an order of the plurality of groups of data may be rearranged within the block of memory, thereby facilitating the further processing of the data according to a butterfly mapping and thereby allowing the decoder to be used to process a trellis of arbitrary size.